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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Noriko SHINOMIYA

Confirmation No. 3304

Serial No.: 10/606,283

Group Art Unit: 2825

Filed: June 26, 2003

Examiner: Nghia M. Doan

For: SEMICONDUCTOR INTEGRATED CIRCUIT DESIGNING APPARATUS, SEMICONDUCTOR INTEGRATED CIRCUIT DESIGNING METHOD, SEMICONDUCTOR INTEGRATED CIRCUIT MANUFACTURING METHOD, AND READABLE RECORDING MEDIA

RESPONSE TO RESTRICTION REQUIREMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action mailed September 27, 2005, applicants hereby provisionally elect, with traverse, to prosecute the claims of Group I (claims 1-4, 9-12, 18 and 22) in this application.

However, applicants respectfully traverse the restriction requirement since the subject matter of all of claims 1-25 are sufficiently related that a thorough and complete search for the subject matter of the elected claims would necessarily encompass a thorough and complete search for the